TL7231MD

FULL LAYER-III ISO/IEC 11172-3 AUDIO DECODER

- Single-chip ISO/IEC 11172-3 Layer III Audio Decoder
- Supports All MPEG Bit Rates Including Free Format
- Supports 32/44.1/48KHz Sampling Frequencies for MPEG Bit Stream
- Supports Single Channel, Dual Channel, Stereo, and Joint Stereo
- Any Combination of Intensity Stereo and MS Stereo is supported.
- Serial Bit Stream Input
- 8-bit Host Interface Port
- Digital Volume Control
- Digital Bass Boost Control
- Voice Record/Playback Capability
- On-chip DAC with 1-bit Sigma Delta Modulation
- Supports Off-chip DAC Interface
- On-chip ADC with 12-bit Resolution
- Supports Off-chip ADC Interface
- Power Management to Reduce Power Consumption
- PLL for Internal Clocks and for Output PCM Clock Generation
- Single 16.9344MHz External Clock Input
- 2.7 V Operation
- Small Footprint 100-pin Thin Quad Flat Package

DESCRIPTION

TL7231MD is a single-chip ISO/IEC 11172-3 Layer III audio decoder, capable of decoding compressed elementary bit streams as specified in ISO/IEC standard. It is designed to be well suited for portable audio appliances.

TL7231MD receives the input data bit stream through a serial data interface. The decoded signal is 16-bit serial PCM format that can be sent directly to DAC. The generated PCM data can be sent to on-chip DAC or off-chip DAC according to user preference. The off-chip DAC interface is programmable to adapt the PCM output of TL7231MD to the most common DACs used on the market.

An 8-bit host interface port is provided to receive control information from and send status information to host. 8-bit microcontrollers such as those of Intel or Motorola can be connected easily.

TL7231MD has the capability of compressing voice signals. It can receive voice signals through on-chip ADC or off-chip ADC according to user preference. The compressed voice signals are transmitted to or received from host through serial data interface. It can also reproduce the voice signals from the compressed voice signals.

FUNCTIONAL BLOCK DIAGRAM

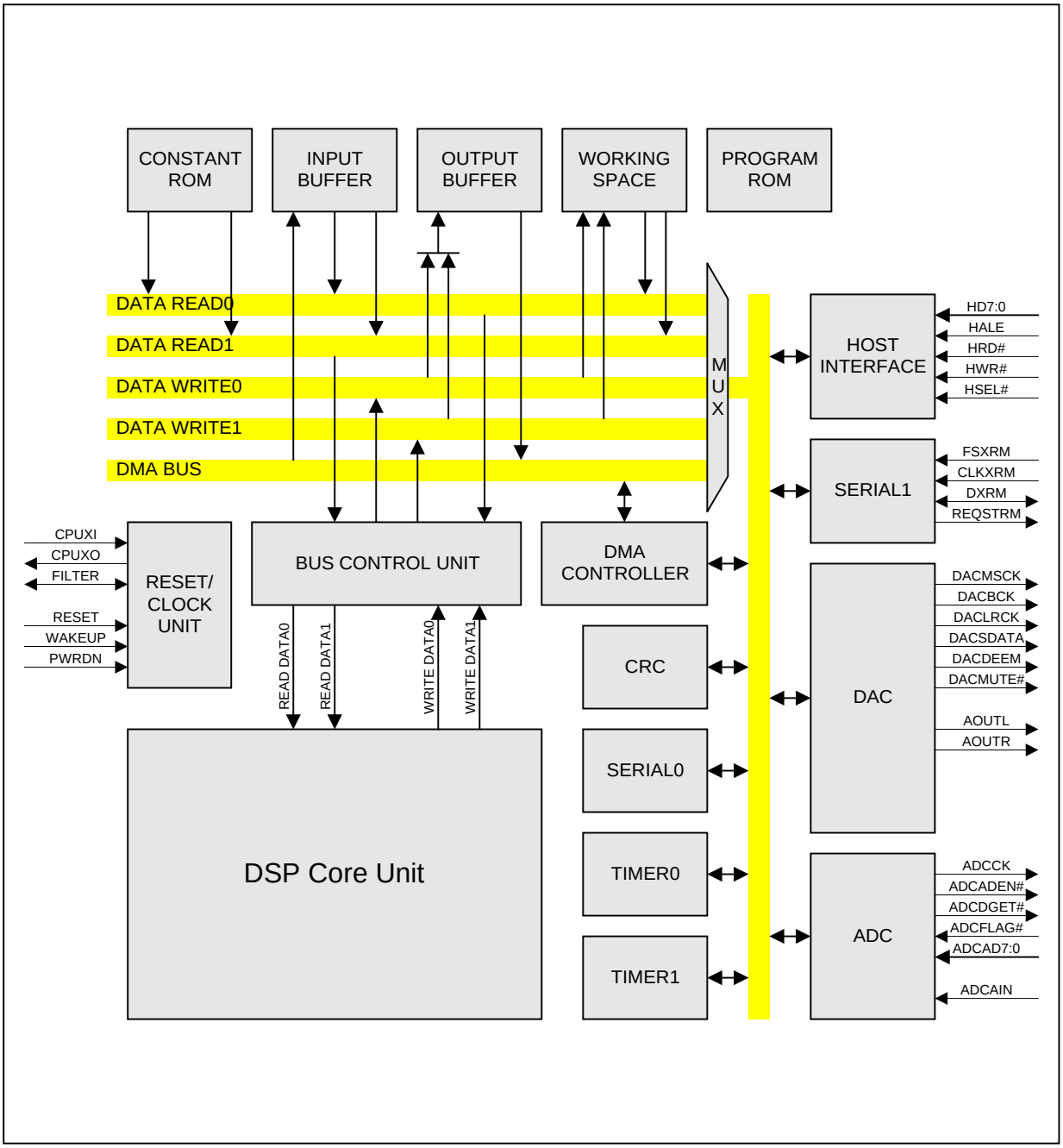


Figure 1. Functional Block Diagram of TL7231MD

PIN DESCRIPTION

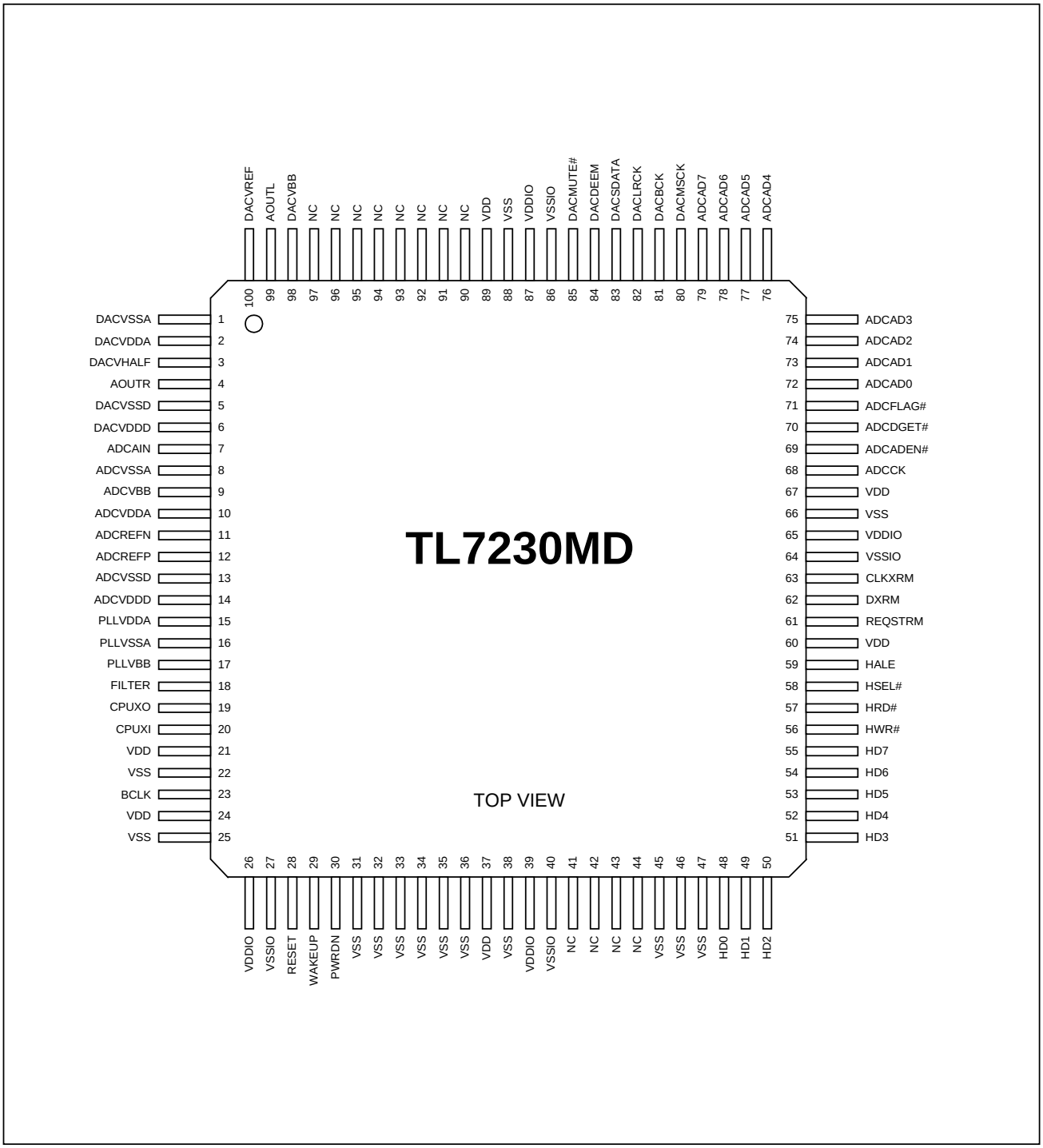


Figure 2. 100-pin Thin Quad Flat Package (TQFP)

Table 1. Pin Locations with Pin Names

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	DACVSSA	26	VDDIO	51	HD3	76	ADCAD4
2	DACVDDA	27	VSSIO	52	HD4	77	ADCAD5
3	DACVHALF	28	RESET	53	HD5	78	ADCAD6
4	AOUTR	29	WAKEUP	54	HD6	79	ADCAD7
5	DACVSSD	30	PWRDN	55	HD7	80	DACMSCK
6	DACVDDD	31	VSS	56	HWR#	81	DACBCK
7	ADCAIN	32	VSS	57	HRD#	82	DACLRCK
8	ADCVSSA	33	VSS	58	HSEL#	83	DACSDATA
9	ADCVBB	34	VSS	59	HALE	84	DACDEEM
10	ADCVDDA	35	VSS	60	VDD	85	DACMUTE#
11	ADCREFN	36	VSS	61	REQSTRM	86	VSSIO
12	ADCREFP	37	VDD	62	DXRM	87	VDDIO
13	ADCVSSD	38	VSS	63	CLKXRM	88	VSS
14	ADCVDDD	39	VDDIO	64	VSSIO	89	VDD
15	PLLVDDA	40	VSSIO	65	VDDIO	90	NC
16	PLLVSSA	41	NC	66	VSS	91	NC
17	PLLVBB	42	NC	67	VDD	92	NC
18	FILTER	43	NC	68	ADCCK	93	NC
19	CPUXO	44	NC	69	ADCADEN#	94	NC
20	CPUXI	45	VSS	70	ADCDGET#	95	NC
21	VDD	46	VSS	71	ADCFLAG#	96	NC
22	VSS	47	VSS	72	ADCAD0	97	NC
23	BCLK	48	HD0	73	ADCAD1	98	DACVBB
24	VDD	49	HD1	74	ADCAD2	99	AOUTL
25	VSS	50	HD2	75	ADCAD3	100	DACVREF

Table 2. Pin Functions with Location

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
ADCAD0	72	CPUXO	19	HRD#	57	VDD	67
ADCAD1	73	DACBCK	81	HSEL#	58	VDD	89
ADCAD2	74	DACDEEM	84	HWR#	56	VDDIO	26
ADCAD3	75	DACLRCK	82	NC	41	VDDIO	39
ADCAD4	76	DACMSCK	80	NC	42	VDDIO	65
ADCAD5	77	DACMUTE#	85	NC	43	VDDIO	87
ADCAD6	78	DACSDATA	83	NC	44	VSS	22
ADCAD7	79	DACVBB	98	NC	90	VSS	25
ADCADEN#	69	DACVDDA	2	NC	91	VSS	31
ADCAIN	7	DACVDDD	6	NC	92	VSS	32
ADCCK	68	DACVHALF	3	NC	93	VSS	33
ADCDGET#	70	DACVREF	100	NC	94	VSS	34
ADCFLAG#	71	DACVSSA	1	NC	95	VSS	35
ADCREFN	11	DACVSSD	5	NC	96	VSS	36
ADCREFP	12	DXRM	62	NC	97	VSS	38
ADCVBB	9	FILTER	18	PLLVBB	17	VSS	45
ADCVDDA	10	HD0	48	PLLVDDA	15	VSS	46
ADCVDDD	14	HD1	49	PLLVSSA	16	VSS	47
ADCVSSA	8	HD2	50	PWRDN	30	VSS	66
ADCVSSD	13	HD3	51	REQSTRM	61	VSS	88
AOUTL	99	HD4	52	RESET	28	VSSIO	27
AOUTR	4	HD5	53	VDD	21	VSSIO	40
BCLK	23	HD6	54	VDD	24	VSSIO	64
CLKXRM	63	HD7	55	VDD	37	VSSIO	86
CPUXI	20	HALE	59	VDD	60	WAKEUP	29

Table 3. Pin Descriptions

Signal Name	Type	Description
Internal PLL Interface		
CPUXI	I	**CPU Clock In.** 16.9344MHz crystal clock input.
CPUXO	O	**CPU Clock Out.** 16.9344MHz crystal clock output.
FILTER	O	**Charge Pump Out.** External capacitor should be connected between this pin and analog ground.
Clock Signal		
BCLK	O	**Processor Clock Output.**
Reset & Power Down Control		
RESET	I	**Chip Reset.** Reset input to the chip. Internal pull down.
WAKEUP	I	**Wake Up.** When high, chip is waked up from SLEEP state. This pin should be remained active at least 1 clock cycle and inactive before the host issues next SLEEP command. Internal pull down.
PWRDN	I	**Power Down.** This pin controls PWRDOWN state. When high, chip goes to very low power consumption state. After deactivation, WAKEUP pin should be remained low at least 150μs. Internal pull down. (Restriction: This pin should be active ONLY in SLEEP state. Otherwise, Chip reset should be activated.)
MCU Serial Interface		
CLKXRM	I	**Serial Clock.** MCU serial interface clock**.**
DXRM	I/O	**Serial Data.** When MCU transmits data, this data pin is sampled at negative edge of CLKXRM. When MCU receives data, Data is valid from negative edge of CLKXRM to next negative edge of CLKXRM. DXRM should be sampled at positive edge of CLKXRM. After reset, TL7231MD is set to transmit the most significant bit first.
REQSTRM	O	**Request Bit Stream Data.** MCU must check this pin to determine to continue receiving or transmitting. MCU should transmit or receive data during this signal active.
MCU HIP(Host Interface Port) Interface		
HSEL#	I	**HIP Enable.** When Low, HIP is selected.
HALE	I	**HIP Address Latch Enable.** When High, HD7:0 should have HIP address, which is sampled at negative edge of this signal.
HRD#	I	**HIP Read Enable.** When low, data is loaded to HD7:0, which should be sampled at positive edge of this signal.
HWR#	I	**HIP Write Enable.** Data at HD7:0 is sampled at positive edge of this signal.
HD7:0	I/O	**HIP Address/Data Bus.** Multiplexed address lines and data lines.
External ADC Interface		
ADCCK	O	**ADC Clock.** External ADC master clock**.**
ADCADEN#	O	**ADC Conversion Enable.** If this signal is activated, analog-to-digital conversion is started.
ADCDGET#	O	**ADC Read Enable.** ADCAD data read enable.
ADCFLAG#	I	**ADC Data Ready.** ADC operation check. Digital state flag.
ADCAD7:0	I	**ADC Digital Data.** Converted PCM data from analog input.

Internal ADC Interface		
ADCAIN	I	**ADC Analog Input.** Analog input spans between ADCREFP and ADCREFN.
ADCREFP	I	**ADC Internal Reference Top Bias**. Connect this pin to voltage between ADCVDDA and 2.0V.
ADCREFN	I	**ADC Internal Reference Bottom Bias.** Connect this pin to ground.
ADCVDDA	PWR	**ADC Supply Voltage for Analog Circuit.** Connect this pin to the +2.7V supply voltage.
ADCVSSA	GND	**ADC Ground for Analog Circuit.** Connect this pin to ground.
ADCVDDD	PWR	**ADC Supply Voltage for Digital Circuit.** Connect this pin to the +2.7V supply voltage.
ADCVSSD	GND	**ADC Ground for Digital Circuit.** Connect this pin to ground.
ADCVBB	GND	**ADC Analog/Digital Bulk Bias.** Connect this pin to ground.
External DAC Interface		
DACMSCK	O	**DAC Master Clock.** 384×Fs clock.
DACBCK	O	**DAC Bit Clock.** 32×Fs clock**.**
DACLRCK	O	**DAC Sample Rate Clock.** Fs clock.
DACSDATA	O	**DAC Serial Data.** Serial data**.**
DACDEEM	O	**DAC Deemphasis.** When deemphasis is on, this signal is high. It can be set/clear through HIP commands.
DACMUTE#	O	**DAC Mute.** Analog output mute. When external DAC is set to mute on, this signal is low. It can be set/clear through HIP commands.
Internal DAC Interface		
AOUTL	O	**Analog Output for Left-Channel.**
AOUTR	O	**Analog Output for Right-Channel.**
DACVHALF	I/O	**DAC Reference Voltage Output for Bypass.**
DACVREF	I/O	**DAC Reference Voltage Output for Bypass.**
DACVDDA	PWR	**DAC Supply Voltage for Analog Circuit.** Connect this pin to the +2.7V supply voltage.
DACVSSA	GND	**DAC Ground for Analog Circuit.** Connect this pin to ground.
DACVDDD	PWR	**DAC Supply Voltage for Digital Circuit.** Connect this pin to the +2.7V supply voltage.
DACVSSD	GND	**DAC Ground for Digital Circuit.** Connect this pin to ground.
DACVBB	GND	**DAC Pad Bulk Bias.** Connect this pin to ground.
Power/Ground Pins		
VDD	PWR	**Supply Voltage.** Connect this pin to the +2.7V supply voltage.
VSS	GND	**Circuit Ground.** Connect this pin to ground.
VDDIO	PWR	**Supply Voltage for I/O Buffers.** Connect this pin to the +2.7V supply voltage.
VSSIO	GND	**Circuit Ground for I/O Buffers.** Connect this pin to ground.

FUNCTIONAL DESCRIPTION

RESET/CLOCK UNIT

TL7231MD is driven by a single clock at the frequency of 16.9344MHz. The clock is derived from an external source or from an industry standard crystal oscillator, generating input frequency of 16.9344MHz. The clock generation unit has a PLL, and all the internal clock signals including internal DAC/ADC clocks are generated with the input clock.

When TL7231MD is in power-on-reset, RESET signal should be active at least 150μs till the internal PLL is stabilized. To reset TL7231MD during normal operation, RESET signal should be active at least 16 cycles.

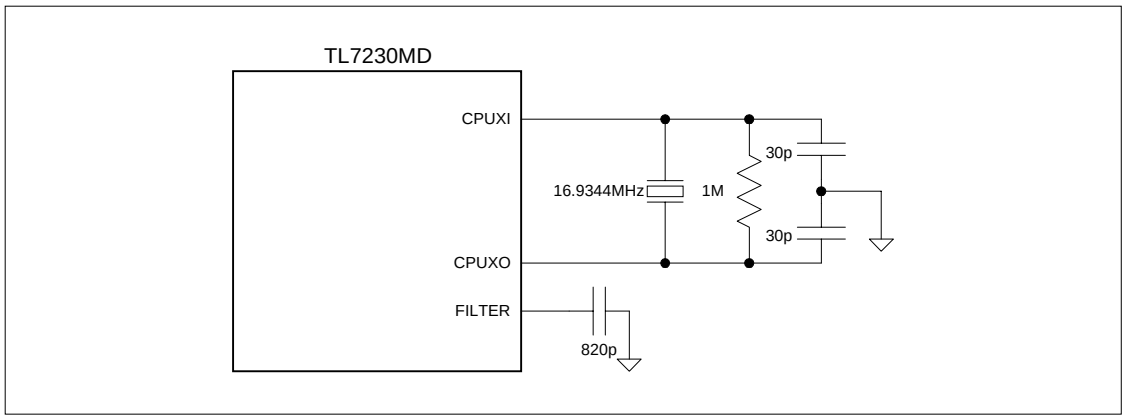


Figure 3. Clock Circuit

DSP CORE LOGIC

The core logic of TL7231MD is a 32-bit floating-point DSP processor. The independent multiplier and accumulator of TL7231MD can achieve high performance. Internal registers are 40-bit registers that store values with a 32-bit mantissa and an 8-bit exponent. These registers can serve as both the source and destination for any arithmetic operation. Since all the data input/output transactions are managed by DMA, there is no computational overhead due to data transactions.

SERIAL INTERFACE

The serial interface of TL7231MD is used to receive MPEG bit stream data or transmit/receive voice data. It is configured to transfer 8 bits of data per word. It can be configured to be LSB-first or MSB first transfer mode. LSB-first means that the data bits are transmitted and received least-significant bit (LSB) first. MSB-first means that the data bits are transmitted and received most-significant bit (MSB) first. The clock for the serial interface should be generated externally.

The related signals are CLKXRM, DXRM, and REQSTRM. REQSTRM is used for synchronization between microcontroller and TL7231MD, and data is transferred during

REQSTRM active.

When microcontroller tries to send data to TL7231MD, it should check whether REQSTRM is active or not. If the signal is active, microcontroller sets its serial interface to transmit mode and send serial clock and serial data. After transmitting each byte, microcontroller should check REQSTRM to decide whether next byte is to be transmitted or not.

When microcontroller tries to receive data from TL7231MD, it should check whether REQSTRM is active or not. If the signal is active, microcontroller sets its serial interface to receive mode and send serial clock and receive serial data from TL7231MD. After receiving each byte, microcontroller should check REQSTRM to decide whether TL7231MD will transmit next byte or not.

HOST INTERFACE PORT (HIP)

Host interface port is used to send commands to and receive status information from TL7231MD. HIP of TL7231MD is a parallel I/O port that makes a connection to a host processor easily. Through the HIP, TL7231MD can be used as a memory-mapped peripheral to a host processor. The HIP can be thought of as an area of dual-port memory that allows communication between the computational core of the TL7231MD and host. The HIP is completely asynchronous. The host processor can write data into the HIP while the TL7231MD is operating at full speed. HIP transfers are managed using interrupt scheme.

HIP contains 21 registers. Four of them are data-in registers (HDI0/HDI1/HDI2/HDI3) and one of them is a status register (HSR4). The remaining 16 registers are data-out registers (HDO0/…/HDO15). Data written into HDIs by host are read by TL7231MD. Through these registers host can give necessary commands to TL7231MD. A command is written into a HDI0, and the required parameters of the command are written into the HDI1/HDI2/HDI3. The status register (HSR4) keeps the information whether data written into the data registers are read by TL7231MD. The status register is managed automatically by TL7231MD and can be read by host. TL7231MD starts HIP command processing when HDI0 register is written. So if any command requires parameters, user should write parameters first, and then write command.

Serial ID number can be used to check whether given command has been accepted or not. TL7231MD writes the serial ID value into HDO0 when TL7231MD has accepted the given command. Thus when commands are given to TL7231MD with different serial ID numbers, it can be examined which command is being processed. Serial ID Number itself hasn't any special meaning. If this feature is not needed, it is not required to send ID values with commands. Then the value of HDO0 is undetermined.

HDOs are written by TL7231MD and can be read by host. All HIP registers should be memory-mapped into the memory space of the host processor. The address space of those registers is shown in Table 4. The usable commands are listed in Table 5. The contents reported by HDOs are shown from Figure 4 to Figure 15.

Table 4. Address of Host Interface Port Registers

ADDRESS	REGISTERS	DESCRIPTION
0x0	HDI0	Command
0x1	HDI1	Serial ID Number
0x2 ~ 0x3	HDI2/HDI3	Parameters if needed
0x4	HSR4	Status Register
0x10	HDO0	Command Serial ID Number
0x11	HDO1	Decoder State
0x12 ~ 0x13	HDO2/HDO3	IO Status
0x14	HDO4	Volume
0x15	HDO5	Serial Interface Mode
0x16 ~ 0x19	HDO6 ~ HDO9	Count
0x1A ~ 0x1C	HDO10 ~ HDO12	The most recently synchronized frame header of MP3 bit stream
0x1D	HDO13	Bass Boost
0x1E	HDO14	DAC Output Valid
0x1F	HDO15	Reserved

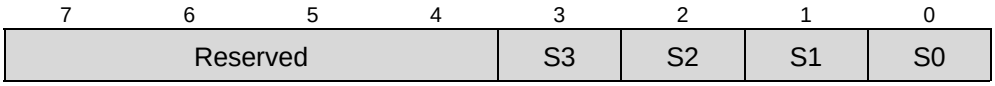
Table 5. Host Interface Port Commands

COMMAND	PARAMETER	MEANING	DESCRIPTION
00h	None	Stop	Stop execution and go into WAIT state.
01h	None	MP3 Decoding	Execute MP3 decoding.
04h	None	Voice Encoding	Execute voice encoding (16Kbps).
05h	None	Voice Decoding	Execute voice decoding (16Kbps).
06h	None	Voice Encoding	Execute voice encoding (24Kbps).
07h	None	Voice Decoding	Execute voice decoding (24Kbps).
08h	None	Voice Encoding	Execute voice encoding (32Kbps).
09h	None	Voice Decoding	Execute voice decoding (32Kbps).
0Fh	None	Sleep	Go into SLEEP state. This command should be used in WAIT state. If this command is used during algorithm execution, TL7231MD becomes unstable.
10h	None	Mute ON	When using internal DAC, The output voltage level of AOUTL/AOUTR is GND. When using external DAC, DACMUTE# becomes active. After reset, TL7231MD is set to be mute on.
11h	None	Mute OFF	Mute off.
12h	None	Internal ADC	Use Internal ADC. External ADC interface is disabled. After reset, it is set to use internal ADC.
13h	None	External ADC	Use external ADC. Analog signal to internal ADC is ignored.
14h	None	Internal DAC	Use internal DAC. After reset, it is set to use internal DAC.
15h	None	External DAC	Use external DAC. Internal DAC is disabled. The waveform of I/O pin related to external DAC is controlled according to External DAC Format or External DAC Format 2.
16h	1byte	External DAC Format†	Set the waveform of I/O pin related to external DAC.
17h	None	MSB First	Serial Interface MSB-first mode. This is the default mode after reset.
18h	None	LSB First	Serial Interface LSB-first mode

20h	1byte	Bass Boost Control (MP3 Only)	Control Bass boost. The upper nibble of the parameter controls the cutoff frequency of bass boost, and the lower nibble controls the level of bass boost. The value of upper nibble should be in the range of 0 to 6. The cutoff frequency is 25×upper nibble + 50 (Hz). If the values of the lower nibble is in the range of 0 to 12, the low frequency band below the cutoff frequency is boosted by 0dB ~ 12dB. The other values mean no boost. †† The reset value is 0xff(disabled).
21h	1byte	Volume Control	Control volume. The parameter should have the value of range from 0 to 200. If the value is *n*, the volume is attenuated by *n*/2 dB compared to maximum volume. The reset value is 0.
8xh	None	External DAC Format2†	Same as External DAC Format command. Parameter values are located at lower nibble of the command.

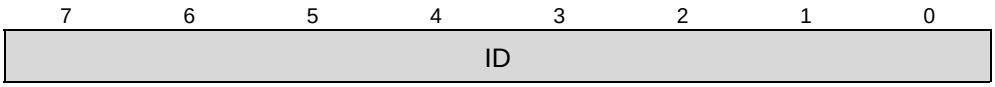
† The parameter value of External DAC Format command should be as follows: {0, 0, 0, 0, 0, I^2S, PL, PB}. For the meaning of I^2S, PL, and PB, refer to Figure 8. For the external DAC format2 command, the command should be {1, 0, 0, 0, 0, I^2S, PL, PB}.

†† In case of using bass boost, volume is reduced by 12dB. For example, if the parameter value is 0x42, then the cutoff frequency will be 25×4+50=150Hz, and the frequency band below 150Hz will be boosted by 2dB compared to the upper frequency band.



Bit Number	Bit Mnemonic	Function
3	S3	When set, it means that host wrote parameter to HDI3 register, but it isn't read by TL7231MD.
2	S2	When set, it means that host wrote parameter to HDI2 register, but it isn't read by TL7231MD.
1	S1	When set, it means that host wrote command ID to HDI1 register, but it isn't read by TL7231MD.
0	S0	When set, it means that host wrote command to HDI0 register, but it isn't read by TL7231MD.

Figure 4. HDI Status Reported through HSR4

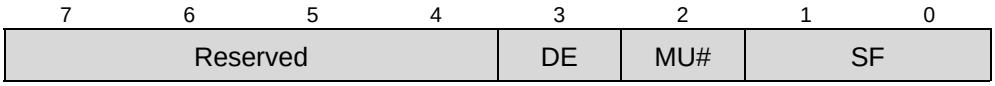


Bit Number	Bit Mnemonic	Function
7:0	ID	Serial ID Number

Figure 5. Command ID reported through HDO0

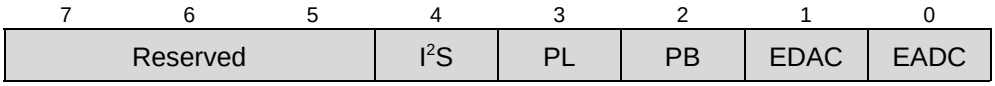
Bit Number	Bit Mnemonic	Function
7:0	STATE	TL7231MD Status Report 0x00: WAIT State 0x01: MP3 Decoding 0x04: Voice Encoding (16Kbps) 0x05: Voice Decoding (16Kbps) 0x06: Voice Encoding (24Kbps) 0x07: Voice Decoding (24Kbps) 0x08: Voice Encoding (32Kbps) 0x09: Voice Decoding (32Kbps)

Figure 6. TL7231MD Status reported through HDO1



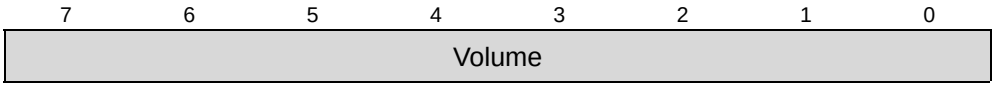
Bit Number	Bit Mnemonic	Function
3	DE	Deemphasis Enable: When set, deemphasis is enabled. Reset value is 0.
2	MU#	Mute Enable: When cleared, mute is on. Reset value is 0.
1:0	FS	Sampling Frequency: During MP3/voice decoding, it shows the sampling frequency of bit stream. DACLRCK is set as follows: 00: 44.1KHz 01: 48KHz 10: 32KHz 11: not used During voice encoding, it shows the sampling frequency of bit stream. ADCADEN# is set as follows: 00: not used 01: not used 10: not used 11: 8KHz Reset value is 00.

Figure 7. I/O Status reported through HDO2



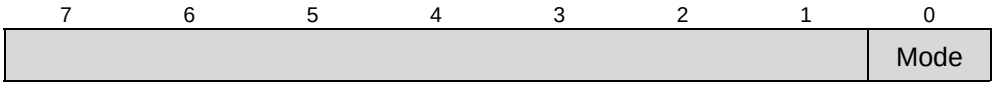
Bit Number	Bit Mnemonic	Function
4	I^2S	I^2S Format Enable: When set, I^2S format (1 bit delay), When cleared normal PCM format. Reset value is 0.
3	PL	Polarity of DACLRCK: When cleared, left channel data is sent through DACSDATA during LRCK=0. When set, right channel data is sent through DACSDATA during LRCK=0. Reset value is 0. (Refer Figure17.)
4	PB	Polarity of DACBCK: When cleared, DACSDATA has valid data between falling edges of DACBCK. When set, DACSDATA has valid data between rising edges of DACBCK. (Refer Figure17.) Reset value is 0.
1	EDAC	External DAC Enable: When set, external DAC is used. Reset value is 0.
0	EADC	External ADC Enable: When set, external ADC is used. Reset value is 0.

Figure 8. I/O Status reported through HDO3



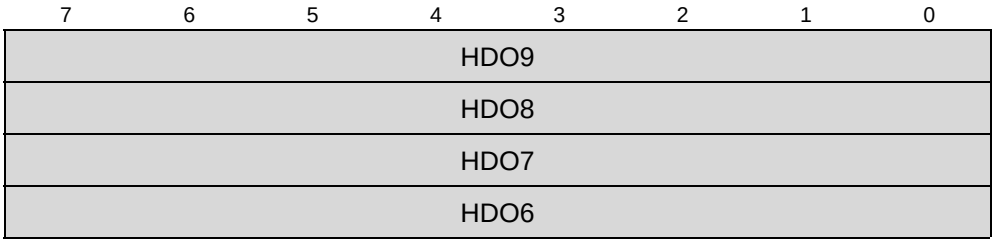
Bit Number	Bit Mnemonic	Function
7:0	Volume	The value can be 0 to 200.

Figure 9. Command ID reported through HDO4



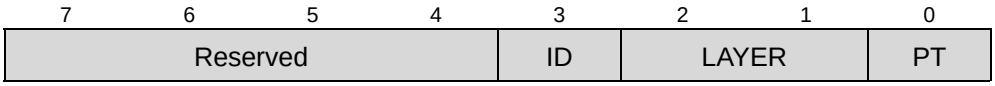
Bit Number	Bit Mnemonic	Function
0	Mode	Serial Interface Mode. When set, LSB-first mode. When cleared, MSB-first mode. The reset value is 0.

Figure 10. Serial Interface Mode reported through HDO5



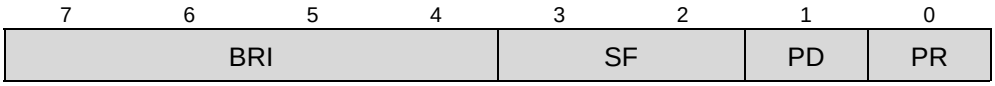
Bit Number	Bit Mnemonic	Function
HDO9 7:0 HDO8 7:0 HDO7 7:0 HDO6 7:0		These registers show 32-bit unsigned integer value. HDO9 is the most-significant byte. For MP3 decoding, it represents the successfully decoded frame counter. For voice encoding/decoding, it represents the encoded/decoded code count.

Figure 11. Count Value reported through HDO6 ~ HDO9



Bit Number	Bit Mnemonic	Function
3	ID	0: Reserved 1: ISO/IEC standard 11172-3 audio (MP3)
2:1	LAYER	00: Reserved 01: Layer3 10: Layer2 11: Layer1 TL7231MD decodes only layer3 bit stream.
0	PT	Protection Bit: 0: CRC Protection 1: No CRC Protection

Figure 12. Frame Header reported through HDO10 (MP3 Only)



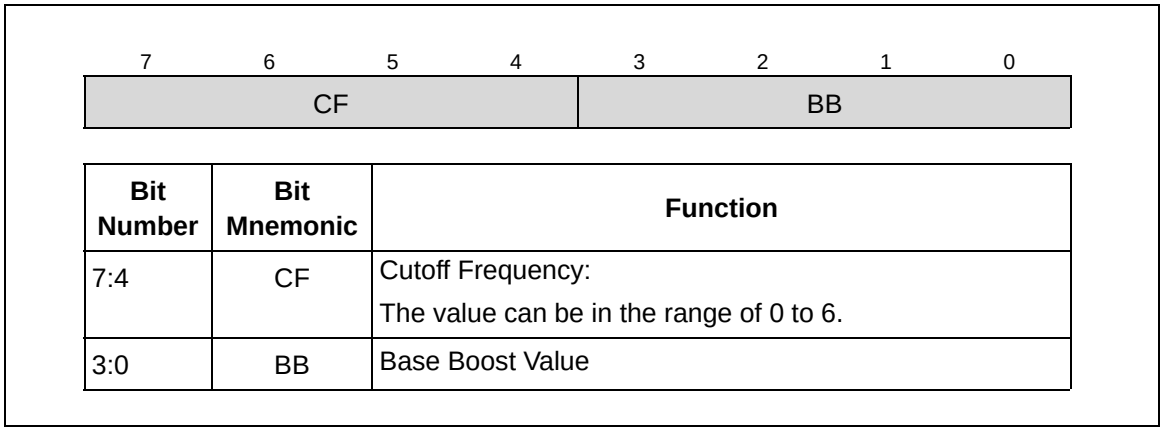
Bit Number	Bit Mnemonic	Function
7:4	BRI	Bit Rate Index: 0000: Free 0001: 32Kbps 0010: 40Kbps 0011: 48Kbps 0100: 56Kbps 0101: 64Kbps 0110: 80Kbps 0111: 96Kbps 1000: 112Kbps 1001: 128Kbps 1010: 160Kbps 1011: 192Kbps 1100: 224Kbps 1101: 256Kbps 1110: 320Kbps 1111: Forbidden
3:2	SF	Sampling Frequency: 00: 44.1KHz 01: 48KHz 10: 32KHz 11: Reserved
1	PD	Padding Bit 0: No Padding Bit 1: One Padding Bit
0	PR	Private Bit Bit for private use.

Figure 13. Frame Header reported through HDO11 (MP3 Only)

7	6	5	4	3	2	1	0
MODE		ME		CR	OC	EM	

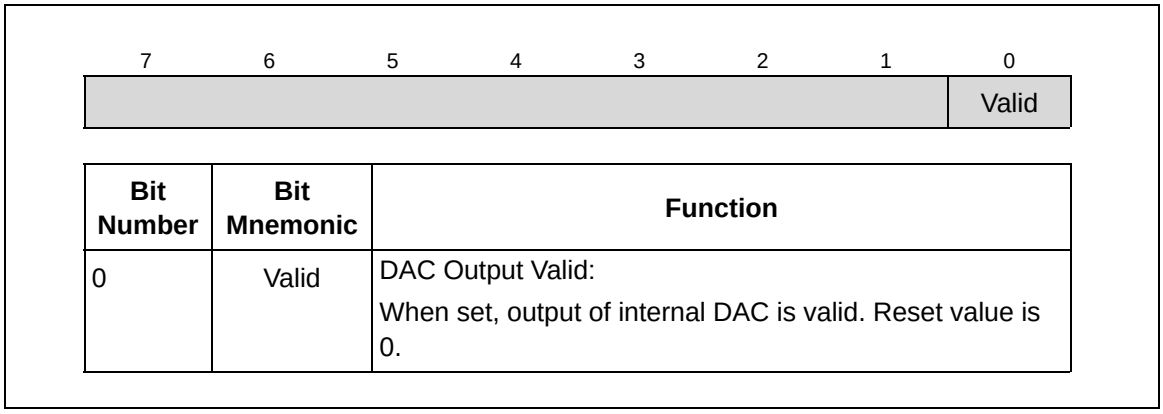
Bit Number	Bit Mnemonic	Function
7:6	MODE	Audio Channel Mode: 00: Stereo 01: Joint Stereo (Intensity Stereo and/or MS Stereo) 10: Dual Channel 11: Single Channel
5:4	ME	Joint Stereo Coding Method: 00: Neither Intensity Stereo nor MS Stereo 01: Only Intensity Stereo 10: Only MS Stereo 11: Both Intensity Stereo and MS Stereo
3	CR	Copyright: 0: No Copyright 1: Copyright Protected
2	OC	Original/Copy: 0: Copy 1: Original
1:0	EM	Type of Deemphasis: 00: None 01: 50/15 microseconds 10: Reserved 11: CCITT J.17 DACDEEM of TL7231MD becomes active if deemphasis is needed without relation to deemphasis type.

Figure 14. Frame Header reported through HDO12 (MP3 Only)



Bit Number	Bit Mnemonic	Function
7:4	CF	Cutoff Frequency: The value can be in the range of 0 to 6.
3:0	BB	Base Boost Value

Figure 15. Serial Interface Mode reported through HDO13 (MP3 Only)



Bit Number	Bit Mnemonic	Function
0	Valid	DAC Output Valid: When set, output of internal DAC is valid. Reset value is 0.

Figure 16. Serial Interface Mode reported through HDO5

DAC

DAC of TL7231MD employs the 1-bit 4th-order sigma-delta architecture with 16-bit resolution, over-sampling of 64X. Analog post-filter with low clock sensitivity and linear phase, filters the shaping-noise and outputs analog voltage with high resolution. The normal input and output channels provides 90dB SNR over in band (20KHz). The characteristic of Internal DAC is shown Table 6.

Table 6. Characteristics of Internal DAC

PARAMETER	MIN	TYP	MAX	UNITS
Resolution		16		bits
SNR	80	90		dB
THD		0.005		%
SND (THD+Noise)		80		dB
Dynamic Range		90		dB
Reference Voltage Output (DACVREF)		0.5× DACVDDA		V
Frequency Responce		± 0.1	± 0.5	dB
Analog Output				
Voltage Range		0.5× DACVDDA		Vpp
Load Impedence	10K			Ω
Digital Filter				
Pass Band Ripple		± 0.0072		dB
Stop and Attenuation		62.7		dB
Pass Band		0.45		Fs

(DACVDDD,DACVDDA=2.4V, Temp=25°C, Fs=44.1KHz, Signal Freq.=20~20KHz, C_{load} of AOUTL,AOUTR = 10pF)

With TL7231MD, user can configure whether the internal DAC is used or not. The configuration of DAC can be achieved through HIP commands shown in Table 5. When using internal DAC, the following circuit in Figure 17 is recommended.

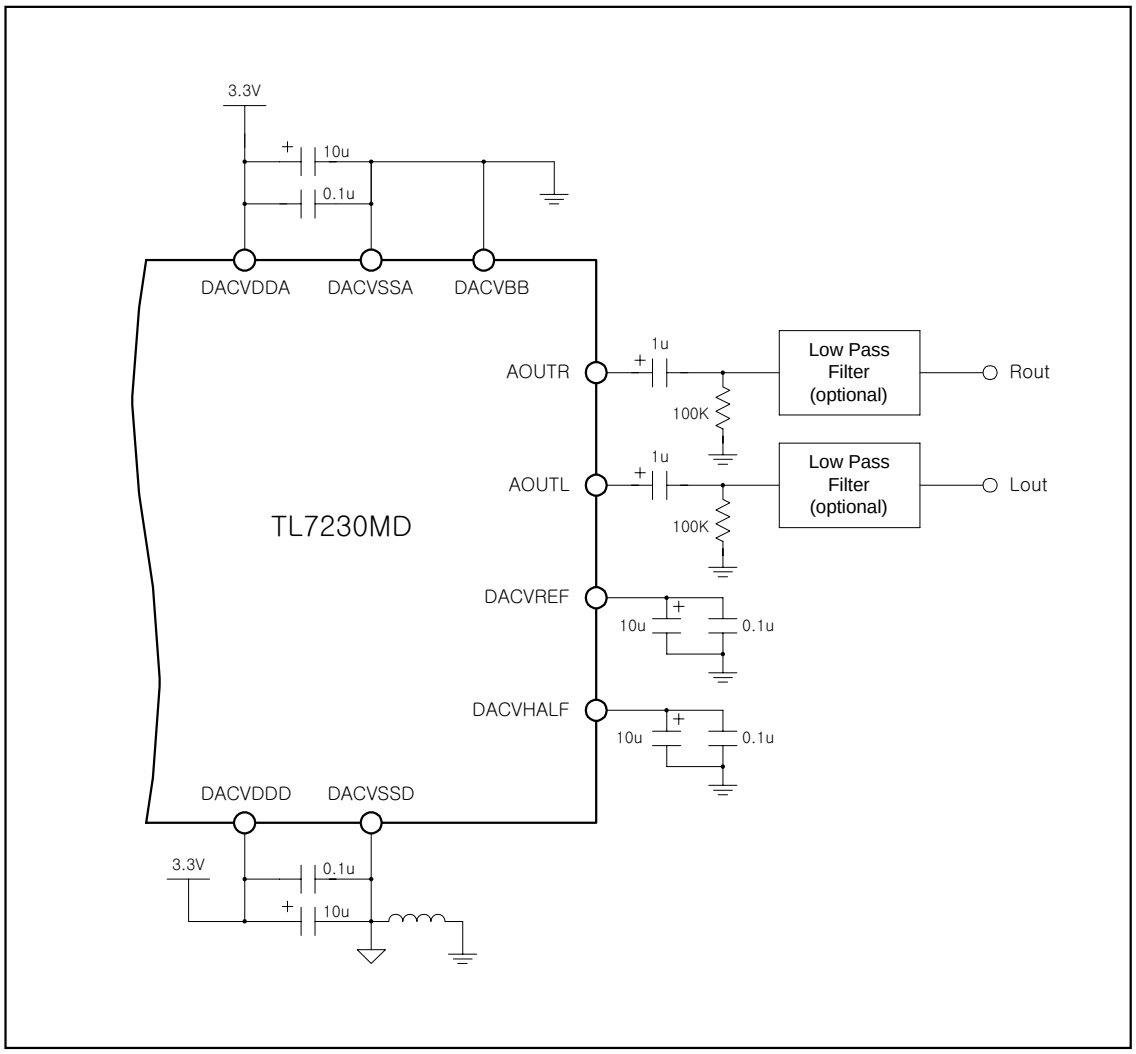


Figure 17. Reference Circuit when using internal DAC

External DAC Interfaces

TL7231MD supports eight external interface formats. Three of them, for example, are shown in Figure 18. The interface can be configured through HIP commands. The frequency of DACBCLK is 32 times of that of DACLRCK. When voice decoding, only 32KHz of DACLRCK of is used.

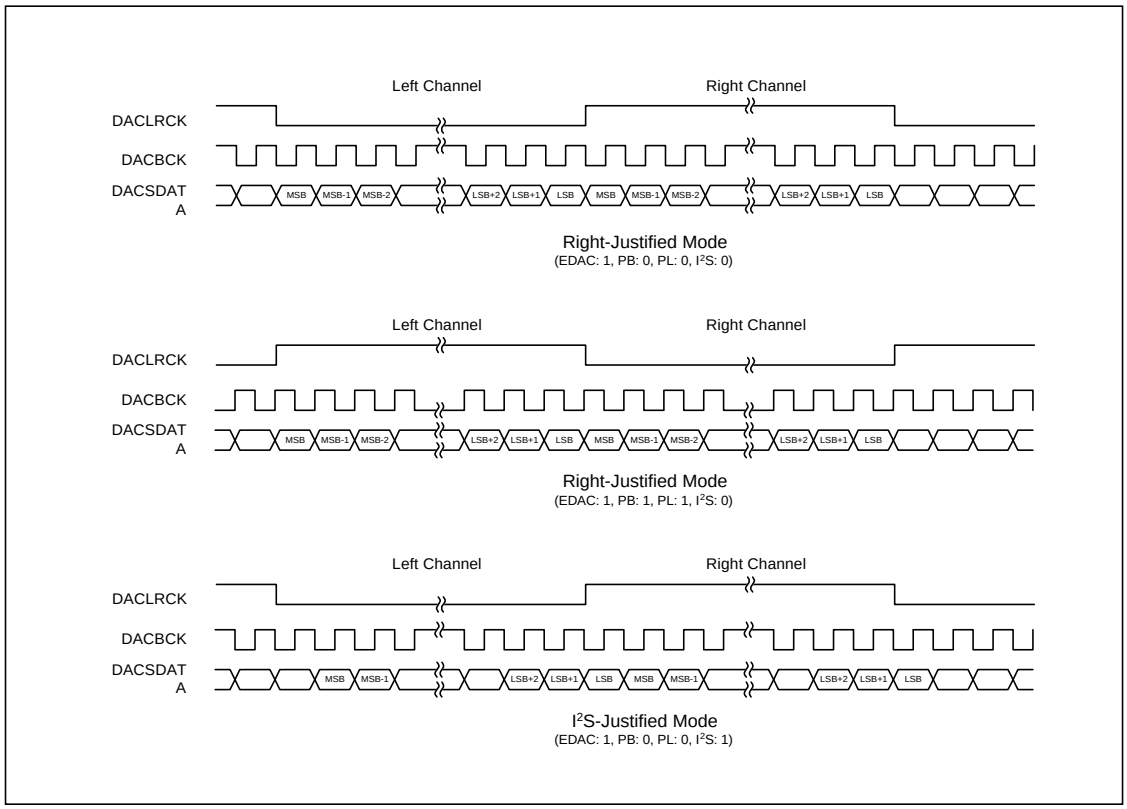


Figure 18. Examples of External DAC Interfaces

ADC

The internal ADC of TL7231MD is 12-bit resolution ADC. It is recycling type ADC with sample-and-hold function. The analog input ADCAIN should be single-ended type with the range from ADCREFP to ADCREFN. This ADCAIN voltage follows reference voltage range fundamentally. So, if user wants to alter the input range, the voltage value of ADCREFP should be changed. But ADCREFP should be greater than 2.0V. The characteristic of Internal ADC is shown Table 7.

Table 7. Characteristics of Internal DAC

PARAMETER	MIN	TYP	MAX	UNITS
THD		-60		dB
SNDR		51		dB

(ADCVDDD,ADCVDDA=3.3V ADCAIN=1KHz)

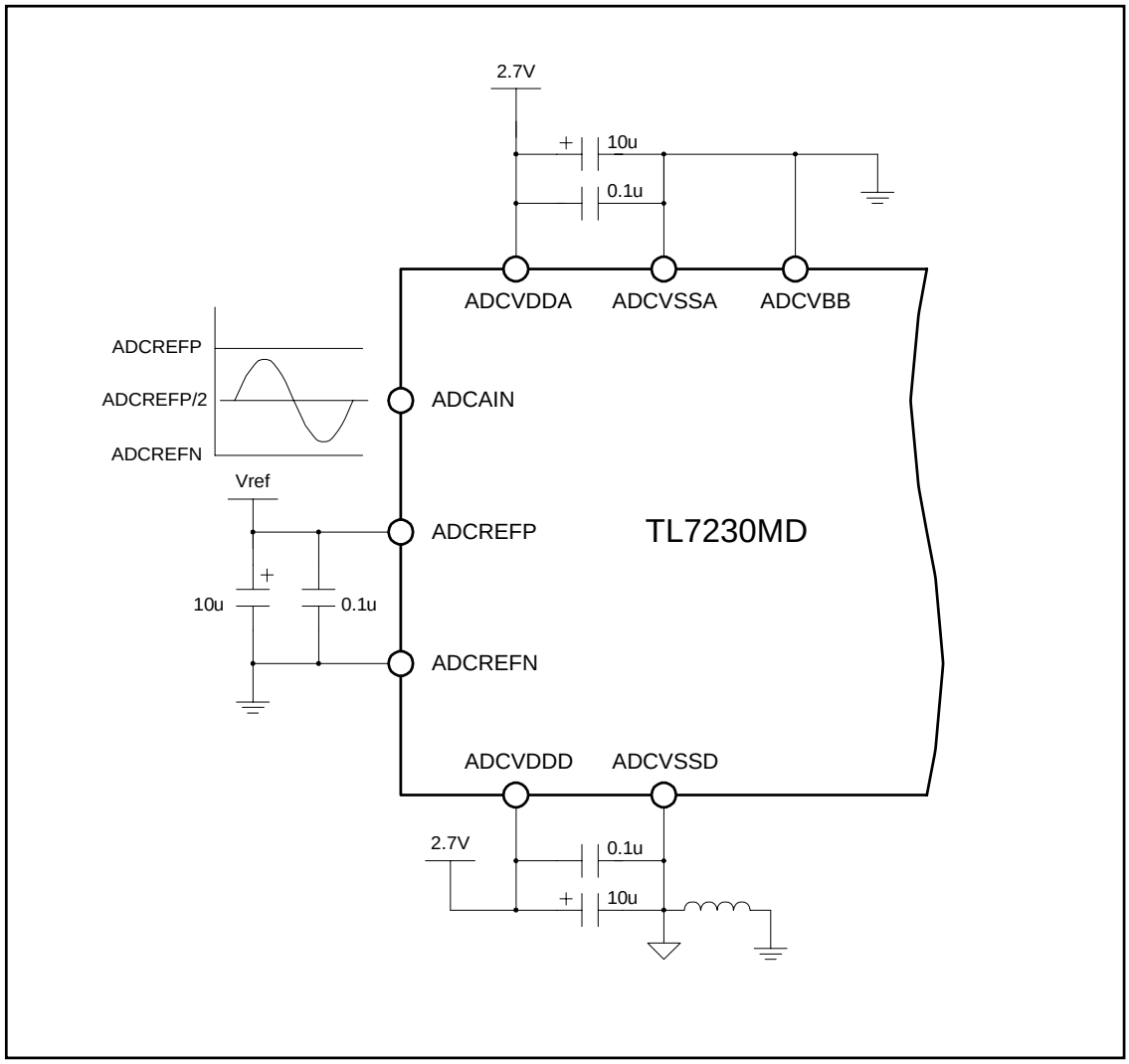


Figure 19. Reference Circuit when using internal ADC

With TL7231MD, user can configure whether the internal ADC is used or not. The configuration of ADC can be achieved through HIP commands shown in Table 5. When using internal ADC,

the following circuit in Figure 19 is recommended.

External ADC Interfaces

External ADC interface scheme is shown in Figure 20. The interface operates as follows. The external ADC starts data conversion when ADCADEN# is low. When the conversion has finished, the external ADC sets ADCFLAG# to low and sends converted data through ADCAD during ADCDGET# is low.

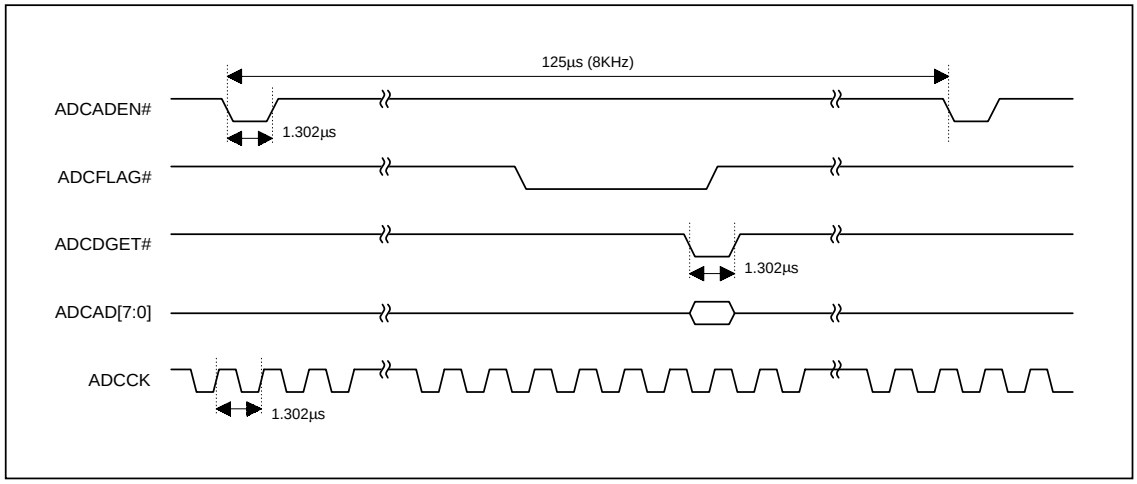


Figure 20. External ADC Interface

Voice Record/Playback Function

TL7231MD records voice data from ADC in 8kHz sampling rate. There are three compression modes according to bit rates of compressed data: high quality (32Kbps), medium quality (24Kbps) and low quality (16Kbps). In high quality mode, relatively large bits are allocated for compressed data to achieve high quality of the sound. In low quality mode, smaller bits are allocated to record much more samples in the same size of storage media. Medium quality mode gives tradeoff between high and low quality modes. Compressed codes are byte-aligned and transmitted to host MCU through the serial port.

In playback the codes are uncompressed to PCM samples, with the compression mode in recording, and then oversampled to 32 kHz and output to DAC. Compressed codes are transmitted from host MCU through the serial interface.

Table 8 is the summary of the relation between compression modes and code size.

Table 8. Summary of Three Voice Compression Modes

COMPRESSION MODES	CODE LENGTH (BIT)	RECORDING TIME FOR 32MB STORAGE MEDIA
High Quality (32Kbps)	4	140 min.
Medium Quality (24Kbps)	3	186 min.
Low Quality (16Kbps)	2	280 min.

Lower Power Operation

TL7231MD has low-power feature that makes the processor get into very low-power dormant states through hardware or software control. The power saving scheme is explained with the state diagram of TL7231MD shown in Figure 21.

RUN

In this state, TL7231MD decodes MP3 or compressed voice bit stream, or encodes voice signal. Also in this state it can process other HIP commands such as 0x20 and 0x21. HIP command 0x01, 0x04 through 0x09, and 0x0F should not be used in this state. TL7231MD consumes normal power at this state, it processes all internal functions and drives external pads. It can transit to WAIT state with HIP command 0x00. When there is no job left or it waits available data, power consumption is reduced as that of WAIT state.

WAIT

When RESET signal becomes active, TL7231MD goes into WAIT state. There it can transit to RUN, or SLEEP state. When TL7231MD is in this state, it is ready to receive any HIP commands from host. It can go into RUN state when it receives HIP commands such as 0x01, 0x04 though 0x09. Also it can process other HIP commands such as volume control (0x21) etc. in this state. TL7231MD goes into this state through HIP command 0x00 from RUN state. When TL7231MD is in this state, only peripheral interface block consumes power. That is, internally generated peripheral clock is active but clock for the DSP core logic is not. When it receives HIP command 0x0F, it goes into SLEEP state in which more power is saved.

SLEEP

In SLEEP state, only internal analog blocks such as PLL, ADC and DAC of TL7231MD consume power. In this state, clocks of internal ADC and DAC are disabled. But PLL consumes normal operation power of about 3.5mA. In this state, TL7231MD can transit to PWRDOWN state when external PWRDN pin becomes active. Active WAKEUP signal changes its state from SLEEP to WAIT.

PWRDOWN

When TL7231MD is in SLEEP state and PWRDN signal becomes active, it transits to PWRDOWN. To make TL7231MD stay in this state, the external PWRDN signal keep its active state. When the PWRDN signal becomes inactive, TL7231MD exits from this PWRDOWN state, and then goes into SLEEP state. When it changes its state from PWRDOWN to SLEEP, this state should not be changed during minimum 150μs until internal PLL is stabilized. TL7231MD consumes the minimum power at this state because all internal logic blocks and analog blocks are power-downed.

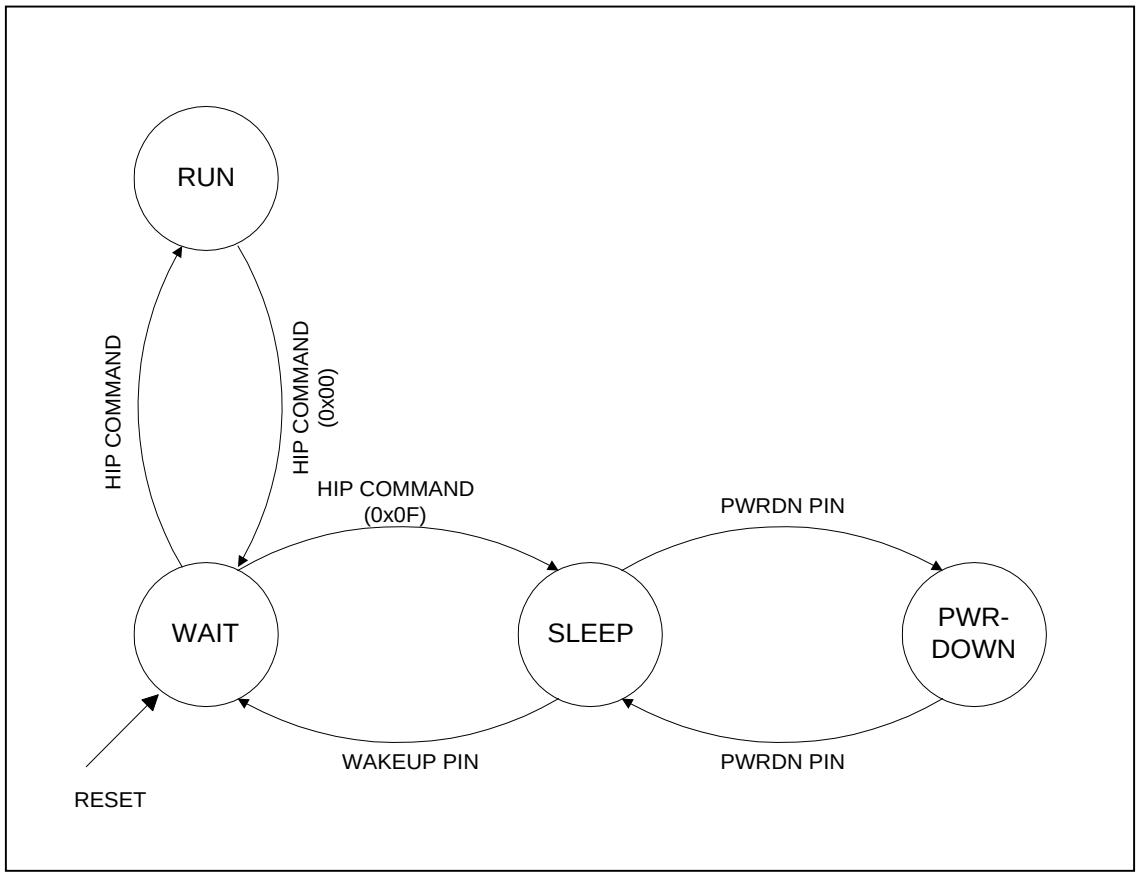


Figure 21. Decoder States and Power Management

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (See Notes)†

Symbol	Parameter	Rating	Unit
V_{DD}	DC Supply Voltage	-0.3 to 3.8	V
V_{IN}	DC Input Voltage	-0.3 to 5.5	V
I_{IN}	DC Input Current	±10	mA
T_{STG}	Storage Temperature	-40 to 125	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “DC ELECTRICAL CHARACTERISTICS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.
NOTE 2: This value was obtained under specially produced worst-case test conditions for the TL7231MD, which are not sustained during normal device operation.

DC ELECTRICAL CHARACTERISTICS (Note3)†

Symbol	Parameter	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	2.4	2.7	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High level input voltage	1.8		V_{DD} +0.3	V
V_{IL}	Low level input voltage	-0.3		0.6	V
V_{OH}	High level output voltage	2			V
V_{OL}	Low level output voltage			0.4	V
I_{IH}	High level input leakage current without internal pull-up	-10		+10	µA
I_{IL}	Low level input leakage current without internal pull-up	-10		+10	µA
I_{RN}	Supply current in RUN state		61		mA
I_{WT}	Supply current in WAIT state		27		mA
I_{SL}	Supply current in SLEEP		13		mA
I_{PD}	Supply current in PWRDOWN state		5.5		µA
C_{IN}	Input capacitance			4	pF
C_{OUT}	Output capacitance			4	pF
T_A	Air temperature	-40		85	°C
V_{CPUXI}	High level input voltage for CPUXI	2.5		V_{DD} +0.3	V

† For TL7231MD, all typical values are at V_{DD} = 2.7 V, T_A (air temperature) = 25°C.

NOTE 3: All voltage values are with respect to V_{SS}. All input and output voltage levels are TTL-compatible. CLKIN can be driven by CMOS clock.

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

AC ELECTRICAL CHARACTERISTICS

AC Test Condition

Parameter	Value
Temperature	85°C
Supply Voltage	2.7V
Input Rise and Fall Times	2ns
Output Load	10pF

Serial port

The following table defines the timing parameters for the serial port pins. The numbers shown in Figure 22 correspond to each number in the first column of the table.

NO.	Symbol	Description	MIN	MAX	Unit
1	T_{CC}	Cycle time of CLKXRM	158.9		ns
2	T_D	Delay time, CLKXRM to DXRM valid	46.3	86.1	ns
3	T_{SU}	Setup time, DXRM before CLKXRM low	2.1		ns
4	T_H	Hold time, DXRM from CLKXRM low	1.3		ns
5	T_{REQ}	Request check time, falling edge of CLKXRM to falling edge of REQSTRM	324.1	363.8	ns

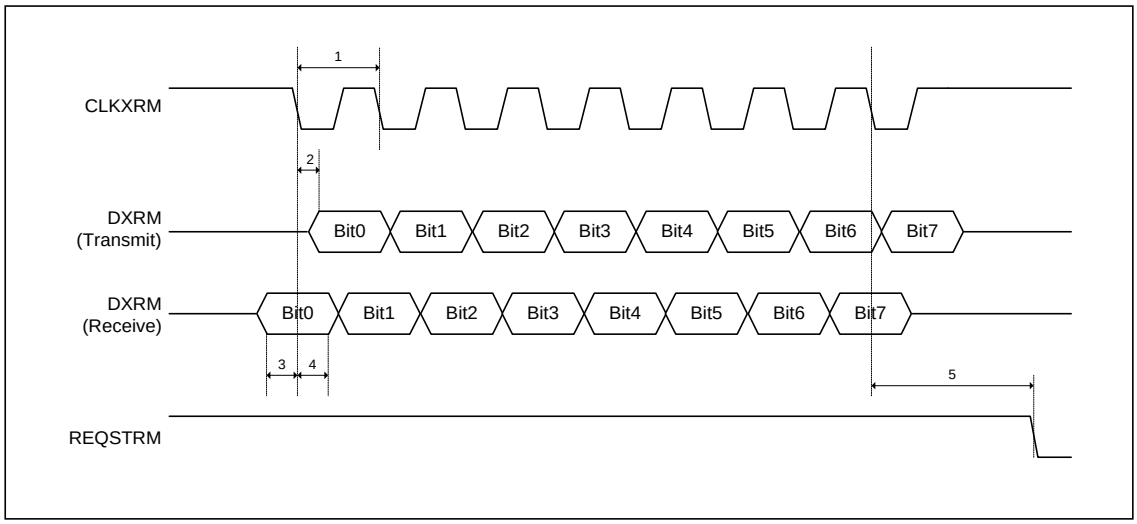


Figure 22. Timing for Serial Port in case of LSB-First Mode

Host interface Port

The following table defines the timing parameters for the Host Interface Port I/O pins. The numbers shown in Figure 23 correspond to each number in the first column of the table.

NO.	Symbol	Description	MIN	MAX	Unit
6	T_{HAW}	HALE pulse width	2.2		ns
7	T_{HDSU}	Setup time, HD address setup before HALE low	2.2		ns
8	T_{HDH}	Hold time, HD address hold after HALE low	0.9		ns
9	T_{HAS}	Start of write or read after HALE low	0.0		ns
10	T_{HDSU}	Setup time, HD data setup before end of write	0.8		ns
11	T_{HDH}	Hold time, HD data hold after end of write	2.4		ns
12	T_{HRW}	Read or write pulse width	39.7		ns
13	T_{HDE}	HD data enabled after start of read	8.6		ns
14	T_{HDD}	HD data valid after start of read	8.7		ns
15	T_{HRDH}	HD data hold after end of read	4.1	8.6	ns
16	T_{HRDD}	HD data disabled after end of read	4.6	8.7	ns

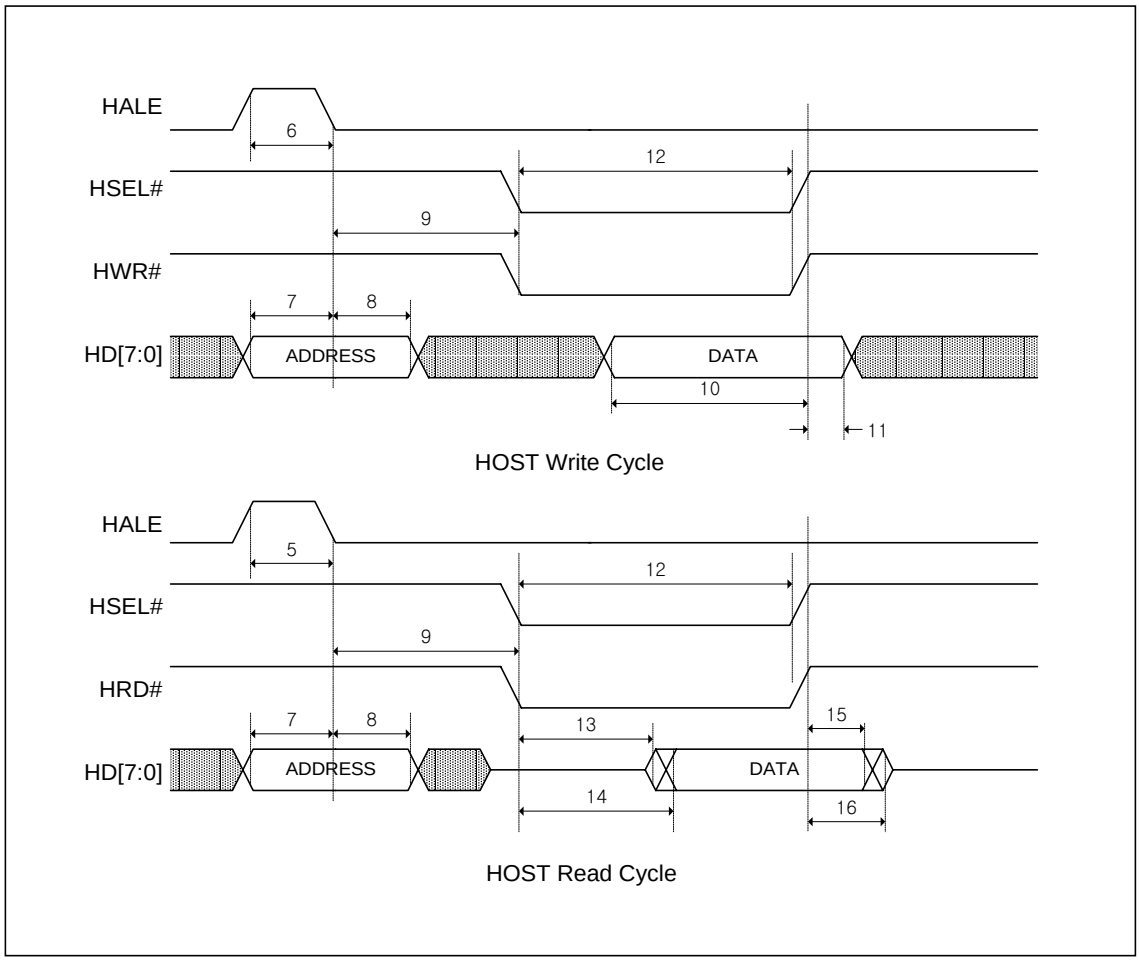


Figure 23. Timing for Host Interface Port pins

External ADC

The following table defines the timing parameters for the external ADC interface pins. The numbers shown in Figure 24 correspond to each number in the first column of the table.

NO.	Symbol	Description	MIN	MAX	Unit
17	T_{CONV}	Conversion time of external ADC		128	μs
18	T_{DFLAG}	Delay from falling edge of ADCFLAG# to falling edge of ADCDGET#	5.7	7.1	μs
19	T_{HDGET}	Hold time, ADCFLAG# hold after ADCDGET# low	0		ns
20	T_{SAD}	Setup time of ADCAD	11.5		ns
21	T_{HAD}	Hold time of ADCAD	0		ns
22	T_{DDGET}	Delay time of the falling edge of ADCDGET# from the falling edge of ADCCK	-0.5	1.0	ns

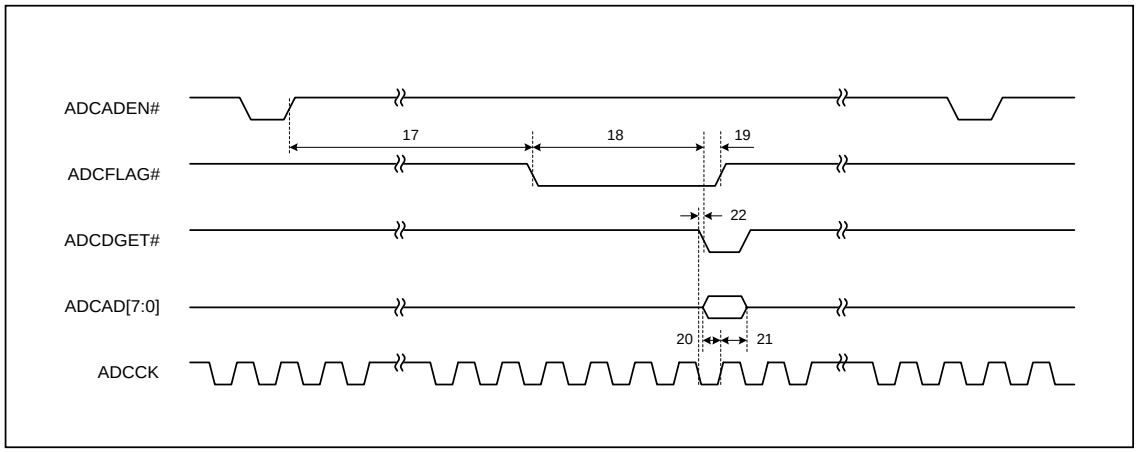


Figure 24. Timing for External ADC Interface pins